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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,977	11/11/2003	Darrell Rinerson	UNTYP029	2976

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,977	RINERSON ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *1-11 and 38-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,20,21,24-26,30-32 and 34* is/are rejected.

7)☒ Claim(s) *13-19,22,23,27-29,33,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/605,977. Currently, claims 1-40 are pending.

Election/Restrictions

2. Applicant's election without traverse of Group I, claims 12-37, in the reply filed on 06 July 2005 is acknowledged. Accordingly, claims 1-11 and 38-40 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

3. Claim 34 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "the plurality of via holes" lacks antecedent basis. To provide antecedent basis for the claim language, claim 34 should depend from claim 33.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu (US 6,569,745 B2).

Hsu discloses a method of making an integrated circuit (figs. 2-6 and accompanying text). The method comprises: providing a semiconductor wafer 12 (fig. 2 and col. 3, lines 1-3); performing front end of line (FEOL) processes on the semiconductor wafer (fig. 2 and col. 2, lines 58-65); forming a plurality of conductive memory devices 17 (25), atop the processed semiconductor wafer, each conductive memory device operable to be reversibly placed in multiple resistive states (fig. 3 and col. 3, lines 11-15); and conducting metallizations 18 after the plurality of conductive memory devices are formed (fig. 4 and col. 3, lines 27-31).

A conducting a first metallization is conducted before the plurality of conductive memory devices are formed (fig. 2 and col. 2, lines 58-64).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Wolf et al. (Silicon Processing for the VLSI Era - Vol. 1: Process Technology).

As discussed above, Hsu discloses a method of making a plurality of conductive memory devices, each conductive memory device operable to be reversibly placed in multiple resistive states. The method comprises: forming a bottom electrode 14, a multi-resistive state element layer 25, and a top electrode layer 18 (see fig. 4), wherein sputtering is one preferred deposition technique used to form the multi-resistive state element layer 25 (col. 3, lines 21-26); and photolithographically patterning the top electrode 18 (col. 3, lines 27-29).

While Hsu discloses the use of a sputtering process to deposit the multi-resistive state element layer, Hsu lacks anticipation of using a sputtering process to form the bottom electrode layer and the top electrode layer.

The Wolf et al. non-patent literature reference (Wolf) teaches that sputtering is a well-known physical vapor deposition technique used to deposit a variety of metallic films in integrated circuit fabrication (see page 335, first paragraph). According to Wolf, sputtering has several advantages. For example, film thickness control is easily achieved (page 335 - second paragraph, item (b)). Secondly, the alloy composition of sputter-deposited films can be more tightly controlled (page 335 - second paragraph, item (c)).

Hsu discloses a method for fabricating a semiconductor circuit, which comprises a plurality of conductive memory devices. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Hsu by using a sputtering technique to form the bottom and top electrode layers, since sputtering is a well-known physical vapor deposition technique used to deposit a variety of metallic films in integrated circuit fabrication.

Again, Hsu discloses the use of a sputtering technique to deposit the multi-resistive state element layer 17 (25). However, Hsu lacks anticipation of depositing the layer using a co-sputtering deposition technique.

Wolf teaches that co-sputtering is a well-known sputtering technique used to deposit alloy films (page 367 - see first paragraph under subheading "Deposition of Alloy Films").

Hsu discloses that the multi-resistive state element layer 17 (25) is a metal oxide alloy film, preferably PCMO (col. 3, lines 14-20). It would have

been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Hsu by depositing the multi-resistive state element layer using a co-sputtering technique, because co-sputtering is a well-known sputtering technique used to deposit alloy films.

Hsu lacks anticipation of a continuous deposition technique to perform at least two of the sputtering processes consecutively. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Hsu and Wolf by using a continuous deposition technique, because with a continuous deposition technique, the sputtering processes are performed in the same sputtering chamber. The transfer of the wafer from one chamber to another is avoided, thereby preventing the growth of a natural oxide layer on the wafer caused by exposure to air.

While Hsu discloses forming the multi-resistive state element layer using a sputtering technique, Hsu lacks anticipation of sputter depositing the layer at less than or equal to about 600°C. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to sputter deposit the multi-resistive state element layer at less than or equal to about 600°C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (see *In re Aller*, 105 USPQ 233).

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Wolf et al. as applied to claim 21 above, and further in view of Newman et al. (US 5,280,013).

Hsu lacks anticipation of using an off-axis sputtering process for at least one of the sputtering processes.

Newman et al. (Newman) teaches a method of forming YBCO on opposites sides of a substrate. One preferred method for forming the YBCO film is off-axis sputtering (col. 4, lines 24-31).

Hsu discloses that in one preferred embodiment, the top and bottom electrode layers are YBCO (col. 3, lines 4-8 and col. 3, lines 27-31). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Hsu and Wolf by using an off-axis sputtering technique to form the bottom and top electrode layers, because off-axis sputtering is a preferred technique used to deposit YBCO films.

7. Claims 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu and Wolf as applied to claim 21 above, and further in view of Wolf (Silicon Processing for the VLSI Era - Vol. 2: Process Integration).

Hsu lacks anticipation of at least one of the bottom and top electrodes including a diffusion barrier layer.

Wolf teaches that it is well known to use diffusion-barrier layers to prevent the intermixing of materials from two layers in contact (). The diffusion barrier layer (1) prevents the diffusion of the two original materials into each other, or (2) resists the tendency of a chemical reaction to form a new phase between the adjoining materials (page 121, first paragraph).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Hsu and Wolf (Vol. 1) by forming at least one of the bottom and top electrodes to include a diffusion barrier layer, because: a diffusion barrier layer prevents the diffusion of the bottom electrode layer/the top electrode layer and the multi-resistive state element layer into each other; and resists the tendency of a chemical reaction to form a new phase between the bottom electrode layer/the top electrode layer and the multi-resistive state element layer.

Allowable Subject Matter

8. Claims 13-19, 22, 23, 27-29, 33, and 35-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The

fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
21 August 2005

Mary Wilczewski
Primary Examiner